REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1-7, 9-13 and 15-20 have been amended as set forth herein.

Claims 1-20 remain pending in this application.

Reconsideration of the claims is respectfully requested. The Applicants have amended Claims 1-7, 9-13 and 15-20 as set forth herein. These amendments add no new matter and are fully supported by the originally-filed Specification. Accordingly, the Applicants respectfully request that the amendments to the claims be entered.

I. CLAIM REJECTION UNDER 35 U.S.C. §102

Claims 1-5 and 7-20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,590,350 to *Guttag, et al.*, hereinafter "*Guttag*". This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-67 (8th ed., rev. 5, August 2006) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

First, Claim 1 of the present application currently requires:

> A method for supporting software pipelining, comprising:
> receiving a *shift mask signal having information on a shifting region of a register file*;
> receiving a shift signal to trigger a shift;
> *identifying a shifting register queue based on the shift mask signal*, wherein the shifting register queue comprises a plurality of queue registers; and
> shifting the contents of the queue registers based on the shift signal. (*emphasis added*).

Guttag, on the other hand, is narrowly directed to a data processing apparatus for computer graphics having three input arithmetic logic unit that form a multi-bit digital signal representing a combination of first, second and third input signals selected by a function signal. *Guttag*, column 3, lines 54-60 and column 5, lines 18-25. A barrel rotator left rotates input data an amount corresponding to a rotate control signal supplies one input signal to the three input arithmetic logic unit. *Id.* at column 5, lines 25-35. At most, *Guttag* teaches using a C-input of the arithmetic logic unit 230 as a mask or merging control. *Id.* at column 61, lines 1-7.

Guttag, however, fails to teach or disclose, for example, *a shift mask signal having information on a shifting region of a register file*, as currently required by independent Claim 1 and its dependents. In addition, *Guttag* fails to teach or disclose, for example, *identifying a shifting register queue based on the shift mask signal*, wherein the shifting register queue comprises a plurality of queue registers, as also currently required by Claim 1 and its dependents.

Similarly, independent Claim 7 of the present application currently requires:

> A system for supporting software pipelining comprising:
> a register file comprising:
> a plurality of queue registers forming *a shifting register queue based on a shift mask signal having information on a shifting region of the register file*; and
> at least one non-queue register located between two queue registers. (*emphasis added*).

Guttag, however, fails to teach or disclose, for example, *a shifting register queue based on a shift mask signal having information on a shifting region of the register file*, as currently required by Claim 7 and its dependents.

Similar arguments exist for independent Claim 13 and its dependents. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to these claims.

II. CLAIM REJECTION UNDER 35 U.S.C. §103

Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Guttag*. The Applicants respectfully traverse the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP §2142, p. 2100-125 (8th ed. rev. 5, August 2006). Absent such a prima facie case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.*

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

Claim 6 depends from allowable Claim 1 and thus is also allowable as shown above. Moreover, *Guttag* dies nit teaching using 0's to identify bits. Moreover, there is no suggestion or motivation within *Guttag* to prompt one of ordinary skill to selectively combine discrete elements from *Guttag* and then *seek out* still others as required by Claim 6.

Accordingly, the Applicants respectfully request the Examiner to withdraw the §103 rejection with respect to Claim 6.